CLAIMS

What is claimed is:

1. A semiconductor component comprising:

a semiconductor substrate;

a first dielectric layer above the semiconductor substrate;

a first ohmic contact region above the semiconductor substrate;

a second ohmic contact region above the semiconductor substrate;

a gate electrode above the semiconductor substrate and between the first ohmic contact region and the second ohmic contact region;

a field plate above the first dielectric layer and between the gate electrode and the second ohmic contact region;

a second dielectric layer above the field plate, the first dielectric layer, the first ohmic contact region, and the second ohmic contact region; and

a third dielectric layer between the gate electrode and the field plate and not located above the gate electrode or the field plate.

2. The semiconductor component of claim 1 wherein:

the third dielectric layer isolates the gate electrode from the field plate.

3. The semiconductor component of claim 1 further comprising:

a semiconductor layer between the semiconductor substrate and the first dielectric layer.

4. The semiconductor component of claim 1 wherein:

the gate electrode comprises a T-gate electrode; and

the T-gate electrode comprises:

a titanium tungsten nitride layer; and

a gold layer above the titanium tungsten nitride layer.

5. The semiconductor component of claim 4 wherein:

a portion of the T-gate electrode overlies at least a portion of the field plate.

6. The semiconductor component of claim 1 wherein:

the gate electrode and the field plate are separated by a distance of between approximately 20 and 400 nanometers.

7. The semiconductor component of claim 1 wherein:

the field plate has a length of between approximately 300 and 2000 nanometers.

8. The semiconductor component of claim 1 wherein:

the field plate comprises titanium tungsten nitride.

9. The semiconductor component of claim 1 wherein:

the first dielectric layer has a thickness of between approximately 50 and 200 nanometers.

10. A method of manufacturing a semiconductor component, the method comprising:

providing a semiconductor substrate;

forming a first dielectric layer above the semiconductor substrate;

forming a field plate above the first dielectric layer; and

self-aligning a gate electrode to the field plate.

11. The method of claim 10 further comprising:

forming a first ohmic contact region and a second ohmic contact region above the semiconductor substrate,

wherein:

self-aligning the gate electrode to the field plate further comprises:

forming the gate electrode after forming the first ohmic contact region and the second ohmic contact region; and

forming the gate electrode to be between the first ohmic contact region and the second ohmic contact region.

12. The method of claim 10 further comprising:

forming a semiconductor layer above the semiconductor substrate before forming the first dielectric layer,

wherein:

forming the first dielectric layer comprises:

forming the first dielectric layer above the semiconductor layer.

13. The method of claim 12 further comprising:

forming a gate recess in the semiconductor layer.

14. The method of claim 10 wherein:

self aligning the gate electrode to the field plate further comprises:

forming a second dielectric layer above the field plate and the first dielectric layer;

forming a hole through the second dielectric layer to expose a portion of the field plate;

removing the portion of the field plate;

removing a portion of the first dielectric layer;

depositing a third dielectric layer over the second dielectric layer and in the hole;

etching the third dielectric layer to form a spacer inside the hole; and

forming the gate electrode in the hole.

15. The method of claim 14 wherein:

forming the second dielectric layer comprises:

forming the second dielectric layer to comprise:

a first tetra-ethyl-ortho-silicate layer;

an aluminum-nitride layer; and

a second tetra-ethyl-ortho-silicate layer.

16. The method of claim 15 wherein:

forming the second dielectric layer further comprises:

forming the aluminum-nitride layer between the first tetra-ethyl-ortho-silicate layer and the second tetra-ethyl-ortho-silicate layer.

17. The method of claim 14 wherein:

forming the gate electrode comprises:

forming a T-gate electrode having a titanium tungsten nitride layer.

18. The method of claim 17 wherein:

forming the T-gate electrode further comprises:

plating a gold layer above the titanium tungsten nitride layer.

19. The method of claim 10 wherein:

forming the first dielectric layer comprises:

forming the first dielectric layer to comprise:

a silicon-nitride layer; and

an aluminum-nitride layer.

20. The method of claim 10 wherein:

forming the gate electrode further comprises:

forming the gate electrode to be separated from the field plate by a distance of between approximately 20 and 400 nanometers.

21. The method of claim 10 wherein:

self-aligning the gate electrode comprises:

shortening a length of the field plate to between approximately 300 and 2000 nanometers.

22. The method of claim 10 wherein:

forming the field plate comprises:

forming the field plate to comprise titanium tungsten nitride.

23. A method of manufacturing a semiconductor component, the method comprising:

providing a semiconductor substrate;

forming a first dielectric layer above the semiconductor substrate;

forming a field plate comprising titanium tungsten nitride above the first dielectric layer;

simultaneously forming a first ohmic contact region and a second ohmic contact region above the semiconductor substrate;

forming a second dielectric layer above the field plate, the first dielectric layer, the first ohmic contact region, and the second ohmic contact region;

forming a hole in the second dielectric layer and between the first ohmic contact region and the second ohmic contact region to expose a portion of the field plate;

removing the portion of the field plate;

removing a portion of the first dielectric layer;

depositing a third dielectric layer over the second dielectric layer and in the hole;

etching the third dielectric layer to form a spacer inside the hole; and

forming a T-gate electrode in and over the hole;

wherein:

the spacer isolates the field plate from the T-gate electrode.

24. The method of claim 23 further comprising:

providing a semiconductor layer above the semiconductor substrate and below the first dielectric layer; and

forming a gate recess in the semiconductor layer,

wherein:

forming the T-gate electrode comprises:

forming the T-gate electrode in the hole and in the gate recess.

25. The method of claim 23 wherein:

forming the T-gate electrode further comprises:

forming the T-gate electrode to be separated from the field plate by a distance of between approximately 20 and 400 nanometers.

26. The method of claim 23 wherein:

forming the field plate comprises:

forming the field plate to have a length of between approximately 300 and 2000 nanometers.

27. The method of claim 23 wherein:

forming the second dielectric layer, forming the hole, removing the portion of the field plate, removing the portion of the first dielectric layer, depositing the third dielectric layer, etching the third dielectric layer, and forming the T-gate electrode comprise self-aligning the T-gate electrode to the field plate.